CET246 Electronic Design Automation
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Laboratory Exercise #2: Single Layer Board Layout

What to do:

1) Unzip the example project into a directory which you have write access to.
2) Open KiCad
3) Open the example project
4) Open the Schematic in Eeschema (within KiCad)
5) Run Pcbnew from the toolbar in EESchema
6) Import the netlist in Pcbnew from the toolbar
7) Arrange the components
8) Make all traces necessary to remove the ratnest. All traces shall be on the **bottom copper layer**.
9) Draw the board edge on the **Edge Cuts** layer. The board shall be no larger than 100mmx 70mm.
10) Include mounting holes
11) Run DRC (bug) check with default design rules and resolve all errors
12) Generate all gerber, drill, and map files as done in the previous lab

What to turn in:

1) A single zip file with all PCB, gerber, drill, and map files. Name the file according to this format:

   Course_Semester_YourLastName_Lab##.zip

   So I would name my file:

   CET246_Fall2018_Broderick_Lab02.zip

